UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,497	09/26/2003	Paul A. Farrar	M4065.0402/P402-C	8623

24998 7590 08/16/2005

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/670,497	FARRAR, PAUL A.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *76-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *76-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 76-83 are rejected under 35 U. S. C. 103(a) as being anticipated by Miyata et al. (US Pat. 6,333,258, herein after Miyata).

Regarding claim 76, Miyata discloses an integrated circuit structure, comprising: a SILK insulating layer 12 (first level) having a thickness of 800nm (8,000Å) (col. 5, lines 10-19) provided over a semiconductor substrate 51/52 and contacting at least a portion of a metal layer 53 provided within semiconductor substrate 51/52; a 800nm (8,000Å) NANOGLASS insulating layer 12 (second level) (col. 17, lines 12-15; col. 17, line 64 through col. 18, line 5; col. 18, lines 59-66) provided over SILK insulating layer 12 (Note that the dielectric 12 comprises SILK 41/ etching stopper 42/NANOGLASS 43) can be "repeated" such that a multilevel wiring layers structure is formed); and a first opening within first insulating layer 12 having a first portion with a first width and a second portion with a second width, first width being different from second width (figs. 2E and 3A-3E); first opening being formed by time etching of first and second

insulating layers 12 with a first etch chemistry (col. 7, lines 18-29). According to the present Specification, page 11, lines 17-20, both the SILK and NANOGLASS layers (k_{SILK} = 2.56 and $k_{NANOGLASS}$ = 3.5 at 100kHz) have a dielectric constant lower than 4.0.

Miyata discloses a 800nm (8,000Å) NANOGLASS insulating layer 12 (col. 17, lines 12-15; col. 17, line 64 through col. 18, line 5; col. 18, lines 59-66) but fails to disclose a NANOGLASS insulating layer having a thickness of 100-2,000Å. It would have been obvious to one with ordinary skill in the art at the time of the invention for forming a NANOGLASS insulating layer having a thickness as taught by Miyata. Although the Miyata range is higher than the claimed range, this does not define patentable over Miyata since the thickness of an insulating layer is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art. The specific thickness of an insulating layer does not provide any critical or unexpected results to an integrated circuit structure. Rather, it is merely an obvious design choice determinable by routine experimentation. In Aller, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

Regarding claim 77, Miyata discloses that the dielectric 12 can be "repeated" such that a third and fourth insulating layers with a dielectric constant lower than 4.0 are necessarily provided over insulating layer 12 (col. 17, lines 12-15); and a second opening within third and fourth insulating layers (multilevel wiring layers), second opening being formed by time etching of third and fourth insulating layers 12 with a second etch chemistry (col. 7, lines 18-29).

Regarding the limitation that the opening being formed by time etching of at least one of SILK and NANOGLASS insulating layers with an etch chemistry (claims 76 and 77), such limitation does not further define the structure as instantly claimed, nor serve to distinguish over Miyata. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw make clear.

Regarding claim 78, Miyata discloses third and fourth insulating layers are formed of different materials which can be selectively etched relative to each other (col. 12, lines 10-17).

Regarding claims 79-83, Miyata discloses third and fourth insulating layers 12 comprise organic/inorganic material (col. 8, line 50 through col. 9, line 47; col. 17, line 64 through col. 18, line 66).

Response to Arguments

2. Applicant's arguments filed 05/25/05 have been fully considered but they are not persuasive.

3. Applicant argues that Miyata does not teach a first insulating layer comprising SILK and the second insulating layer comprising NANOGLASS. Note that Miyata discloses the multilevel wiring layers structure comprising multilevel insulating layer 12 on top of each other (col. 17, lines 12-15); wherein each insulating layer 12 (fig. 3A) comprising SILK 41(col. 8, lines 57-67) / etching stopper 42(col. 14, lines 33-36) / NANOGLASS 43 (col. 18, lines 59-66). The opening being formed by time etching of SILK and NANOGLASS insulating layers with an etch chemistry to provide the wiring groove 24 (col. 7, lines 17-29).

Miyata discloses a 800nm (8,000Å) NANOGLASS insulating layer 12 (col. 17, lines 12-15; col. 17, line 64 through col. 18, line 5; col. 18, lines 59-66) but fails to disclose a NANOGLASS insulating layer having a thickness of 100-2,000Å. Note that the thickness of an insulating layer is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art. The specific thickness of an insulating layer does not provide any critical or unexpected results to an integrated circuit structure. Rather, it is merely an obvious design choice determinable by routine experimentation. In Aller, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995). Moreover, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1.936 (Fed. Cir. 1990). As such, applicant's argument that the thickness of the "second insulating layer" is critical for the time etch process

is not persuasive.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Vu

August 14, 2005